~~an output port for coupling to an input of the read data port primitive~~.

39. (Original in RCE) The memory model of Claim 37, wherein the read data port primitive represents a read port functionality of the memory.

40. (Currently Amended) The memory model of Claim 39, ~~wherein the read data port primitive includes:~~

~~a read enable port;~~

~~a read_address port for coupling to the address bus primitive;~~

~~a read_data port for coupling to the memory primitive; and~~

~~an output port for coupling to the plurality of memory out primitives~~, wherein a dimension of the output port of the read data port corresponds to a data dimension of the memory primitive.

41. (Original in RCE) The memory model of Claim 37, wherein the address bus primitive represents an address functionality of a memory.

42. (Currently Amended) The memory model of Claim 41, wherein the address bus primitive includes:

a plurality of input ports corresponding to an address dimension of the memory primitive~~; and~~

~~an output port for coupling to the memory primitive and the read data port primitive~~.

43. (Original in RCE) The memory model of Claim 42, wherein the address bus primitive further includes an attribute indicating whether an incoming address is encoded or decoded.

44. (Original in RCE) The memory model of Claim 43, wherein the data bus primitive represents a data bus functionality of the memory.

45. (Currently Amended) The memory model of Claim 44, wherein the data bus includes:

a plurality of input ports corresponding to a data dimension of the memory primitive~~; and~~

~~an output port for coupling to the memory primitive~~.

46. (Original in RCE) The memory model of Claim 37, wherein each memory out primitive represents a simulated value storage functionality of the memory.

47. (Currently Amended) The memory model of Claim ~~46~~ 37, wherein each memory out primitive includes~~:~~

~~an input port; and~~

an output port.

48. (Currently Amended) The memory model of Claim ~~37~~ 47, wherein a plurality of tristate drivers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

49. (Currently Amended) The memory model of Claim ~~37~~ 47, wherein a plurality of edge-triggered registers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

50. (Currently Amended) The memory model of Claim 49, wherein input ports of a plurality of tristate drivers can be

coupled to output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive.

51. (Currently Amended) A content addressable memory model usable for simulation and automatic test pattern generation, the content addressable memory model comprising:

a memory primitive including an output port;

a compare port primitive including a data port for coupling to ~~an~~ the output port of the memory primitive, a data bus port, and an output port;

~~an address bus primitive for coupling to the memory primitive and the compare port primitive;~~

a data bus primitive including an output port for coupling to the data bus port of the ~~memory~~ compare port primitive; ~~and~~

a plurality of memory output primitives, each memory output primitive including an input port for coupling to the output port of the compare port primitive and an output port; and

an address bus primitive including input ports for coupling the output ports of a set of the memory output primitives.

52. (Currently Amended) The content addressable memory model of Claim 51, wherein the compare port primitive further includes:

a compare enable port for receiving a compare signal~~,~~

~~a data bus port for coupling to an output port of the data bus primitive;~~

~~a data port for coupling to an output port of the memory primitive; and~~

~~an output port for coupling to input ports of the plurality of memory output primitives~~.

53. (Currently Amended) A combined content addressable memory (CAM) and random access memory (RAM) model usable for simulation and automatic test pattern generation, the combined CAM and RAM model comprising:

a first memory primitive including an output port;

a data bus primitive including an output port;

a compare port primitive for coupling to the memory primitive and the data bus primitive, the compare port primitive comprising;

a compare enable port;

a data bus port for coupling to the output port of the data bus primitive;

a data port for coupling to the output port of the first memory primitive; and

an output port;

a first plurality of memory output primitives, each memory output primitive including an output port and an input port for coupling to the output port of the compare port primitive;

an address bus primitive including an output port and input ports for coupling to output ports of a first subset of the first plurality of memory output primitives;

a second memory primitive including an output port;

a read data port primitive including a first input port for coupling to the output port of the second memory primitive, a second input port for coupling to an output port of the address bus primitive, and a third input port for coupling to the output ports of a second subset of the plurality of memory output primitives; and

a second plurality of memory output primitives, each memory output primitive including an input port for coupling to an output port of the read data port primitive.

54. (Cancelled)

55. (Previously Amended) A memory model compatible with a simulation tool and an automatic test pattern generation (ATPG) tool, the memory model including:

a plurality of primitives, each primitive representing a defined functionality of a memory.

56. (Original in RCE) The memory model of Claim 55, wherein each primitive usable by the ATPG tool is configured based on a subset of behavioral hardware description language (HDL) usable by the simulation tool.

57. (Original in RCE) The memory model of Claim 56, wherein the behavioral HDL includes Verilog.

58. (Original in RCE) The memory model of Claim 56, wherein the subset of behavioral HDL can directly map to the plurality of primitives.